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## Sept Generations DExecuteurs 1688-1847 Memoires Des Sanson MIS En Ordre (2)

By -

RareBooksClub. Paperback. Book Condition: New. This item is printed on demand. Paperback. 66 pages. Original publisher: Aberdeen Proving Ground, MD : Army Research Laboratory, 1999 OCLC Number: (OCOLOC)311097378 Subject: Computational fluid dynamics. Excerpt: . . . This report will discuss how this effect was SGI Power Challenge and the ConvexExemplar approached, what the results were, and the reasons for those results. 2. The Architecture of the SGI Power Challenge Before we can discuss the results of this effort, it is helpful to have a short introduction to the architecture involved. The SGI PowerC challenge and the thought of fast prototypical RISC-based cache-coherence are memory SMP. As such, it will be discussed first. From the hardware perspective, it has the following properties: (1) Powerful RISC-based processors. In this case, RISC processors are rated at 300 MFLOPS each. (2) This version of the PowerC challenge had up to 18 processors and up to 16 GB of memory, although it couldn't configure a system with both 18 processors and 16 GB of memory. (3) Each processor had a large off-chip cache (4 MB). (4) Hardware protocols maintained coherence between...



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